Field of application

This application note details the handshaking procedure to initiate a cyclic data transfer between the MBCCL slave and a CC-Link master PLC and the format of the cyclic process data.

The procedure to implement the handshake on the PLC is out of the scope of this document, please refer to the PLC user manual or support.

System area initial handshake

In order to start the cyclic exchange the PLC has to handle the System Area as following:

- react to a set "Initial Data Processing Request"-flag by setting the "Initial Data Processing Complete"-flag. The Complete Flag should be reset as soon as the Request is reset;
- set the "Initial Data Setting Request"-flag until the "Initial Data Setting Complete"- and the "Remote READY"-flag are set.

Every time the connection gets interrupted, the PLC has to wait for the "Initial Data Processing Request"-flag again.

System area			
Slave -> Master		**Master -> Slave**	
Point	**Contents**	**Point**	**Contents**
RX #0	Not used	RY #0	Not used
RX #1		RY #1	
…		…	
RX #12E		RY #12E	
RX #12F		RY #12F	
RX #130	Reserved	RY #130	Reserved
RX #131		RY #131	
RX #132		RY #132	
RX #133		RY #133	
RX #134		RY #134	
RX #135		RY #135	
RX #136		RY #136	
RX #137		RY #137	
RX #138	Initial Data Processing Request	RY #138	Initial Data Processing Complete
RX #139	Initial Data Setting Complete	RY #139	Initial Data Setting Request
RX #13A	Error Status	RY #13A	Error Reset Request
RX #13B	Remote READY	RY #13B	Reserved
RX #13C	Reserved	RY #13C	
RX #13D		RY #13D	
RX #13E		RY #13E	
RX #13F		RY #13F	

Process data mapping

Data in the MBCCL is accessed as 16-bit words. The MBCCL is set CC-Link version 2, 3 Occupied Stations, 4 Extension Cycles.
The process data are described in the folowing tables.

Master -> Slave		
Point	**Contents (MSB)**	**Contents (LSB)**
RWw #0	Fieldbus input byte 1	Fieldbus input byte 0
RWw #1	Fieldbus input byte 3	Fieldbus input byte 2

Slave -> Master		
Point	**Contents (MSB)**	**Contents (LSB)**
RWr #0	Reserved	System status
RWr #1	Input status byte 02	Input status byte 01
RWr #2	Input status byte 04	Input status byte 03
RWr #3	Input status byte 06	Input status byte 05
RWr #4	Input status byte 08	Input status byte 07
RWr #5	Input status byte 10	Input status byte 09
RWr #6	Input status byte 12	Input status byte 11
RWr #7	Input status byte 14	Input status byte 13
RWr #8	Input status byte 16	Input status byte 15
RWr #9	Fieldbus input feedback byte 1	Fieldbus input feedback byte 0
RWr #10	Fieldbus input feedback byte 3	Fieldbus input feedback byte 2
RWr #11	Probe status byte 1	Probe status byte 0
RWr #12	Probe status byte 3	Probe status byte 2
RWr #13	OSSD status byte 1	OSSD status byte 0
RWr #14	OSSD status byte 3	OSSD status byte 2
RWr #15[1]	Analog data float 0 (bit 8-15)	Analog data float 0 (bit 0-7)
RWr #16	Analog data float 0 (bit 24-31)	Analog data float 0 (bit 16-23)
RWr #17	Analog data float 1 (bit 8-15)	Analog data float 1 (bit 0-7)
RWr #18	Analog data float 1 (bit 24-31)	Analog data float 1 (bit 16-23)
RWr #19	Analog data float 2 (bit 8-15)	Analog data float 2 (bit 0-7)
RWr #20	Analog data float 2 (bit 24-31)	Analog data float 2 (bit 16-23)
RWr #21	Analog data float 3 (bit 8-15)	Analog data float 3 (bit 0-7)
RWr #22	Analog data float 3 (bit 24-31)	Analog data float 3 (bit 16-23)
RWr #23	Analog data float 4 (bit 8-15)	Analog data float 4 (bit 0-7)
RWr #24	Analog data float 4 (bit 24-31)	Analog data float 4 (bit 16-23)
RWr #25	Analog data float 5 (bit 8-15)	Analog data float 5 (bit 0-7)
RWr #26	Analog data float 5 (bit 24-31)	Analog data float 5 (bit 16-23)
RWr #27	Analog data float 6 (bit 8-15)	Analog data float 6 (bit 0-7)
RWr #28	Analog data float 6 (bit 24-31)	Analog data float 6 (bit 16-23)
RWr #29	Analog data float 7 (bit 8-15)	Analog data float 7 (bit 0-7)
RWr #30	Analog data float 7 (bit 24-31)	Analog data float 7 (bit 16-23)
RWr #31	Analog data float 8 (bit 8-15)	Analog data float 8 (bit 0-7)
RWr #32	Analog data float 8 (bit 24-31)	Analog data float 8 (bit 16-23)
RWr #33	Analog data float 9 (bit 8-15)	Analog data float 9 (bit 0-7)
RWr #34	Analog data float 9 (bit 24-31)	Analog data float 9 (bit 16-23)
RWr #35	Analog data float 10 (bit 8-15)	Analog data float 10 (bit 0-7)
RWr #36	Analog data float 10 (bit 24-31)	Analog data float 10 (bit 16-23)
RWr #37	Analog data float 11 (bit 8-15)	Analog data float 11 (bit 0-7)
RWr #38	Analog data float 11 (bit 24-31)	Analog data float 11 (bit 16-23)
RWr #39	Analog data float 12 (bit 8-15)	Analog data float 12 (bit 0-7)
RWr #40	Analog data float 12 (bit 24-31)	Analog data float 12 (bit 16-23)
RWr #41	Analog data float 13 (bit 8-15)	Analog data float 13 (bit 0-7)
RWr #42	Analog data float 13 (bit 24-31)	Analog data float 13 (bit 16-23)
RWr #43	Analog data float 14 (bit 8-15)	Analog data float 14 (bit 0-7)
RWr #44	Analog data float 14 (bit 24-31)	Analog data float 14 (bit 16-23)
RWr #45	Analog data float 15 (bit 8-15)	Analog data float 15 (bit 0-7)
RWr #46	Analog data float 15 (bit 24-31)	Analog data float 15 (bit 16-23)
RWr #47[2]	Error Code[MSB]	Error Code[LSB]

[1] Please note that the presence of the Analog data depends on the MBCCL configuration.

[2] If the Analog data are not selected in the configuration the Error code address will be RWr #15 instead of RWr #47.